High-level Partitioning Of Discrete Signal Transforms For Distributed Hardware Architectures

By: Rafael Arce-Nazario, PhD Student

Advisor:
Prof. Manuel Jiménez

WALSAIP

Automated Information Processing Laboratory (AIP)
University of Puerto Rico, Mayagüez Campus (UPRM)
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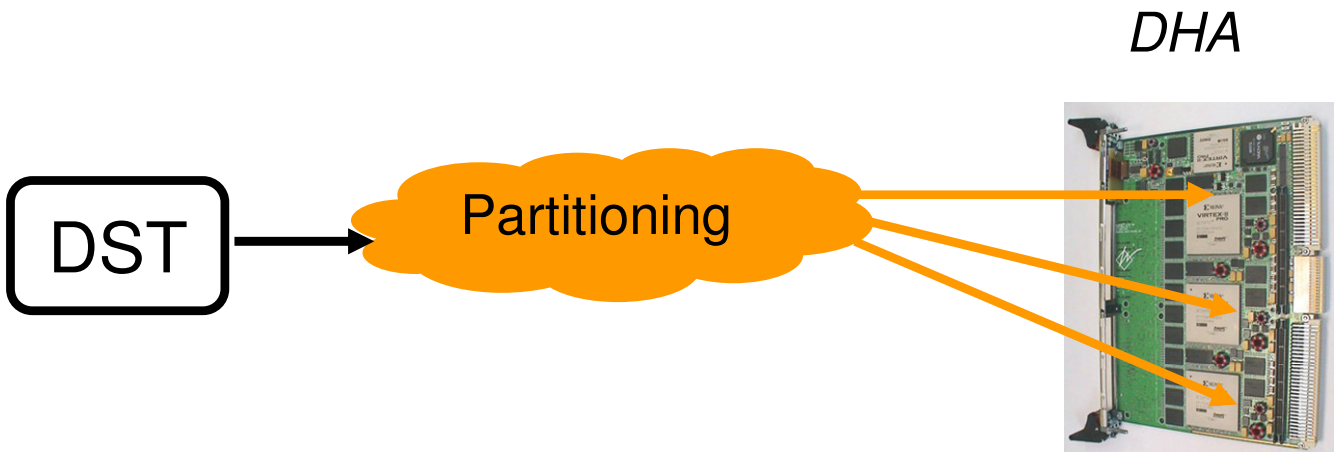
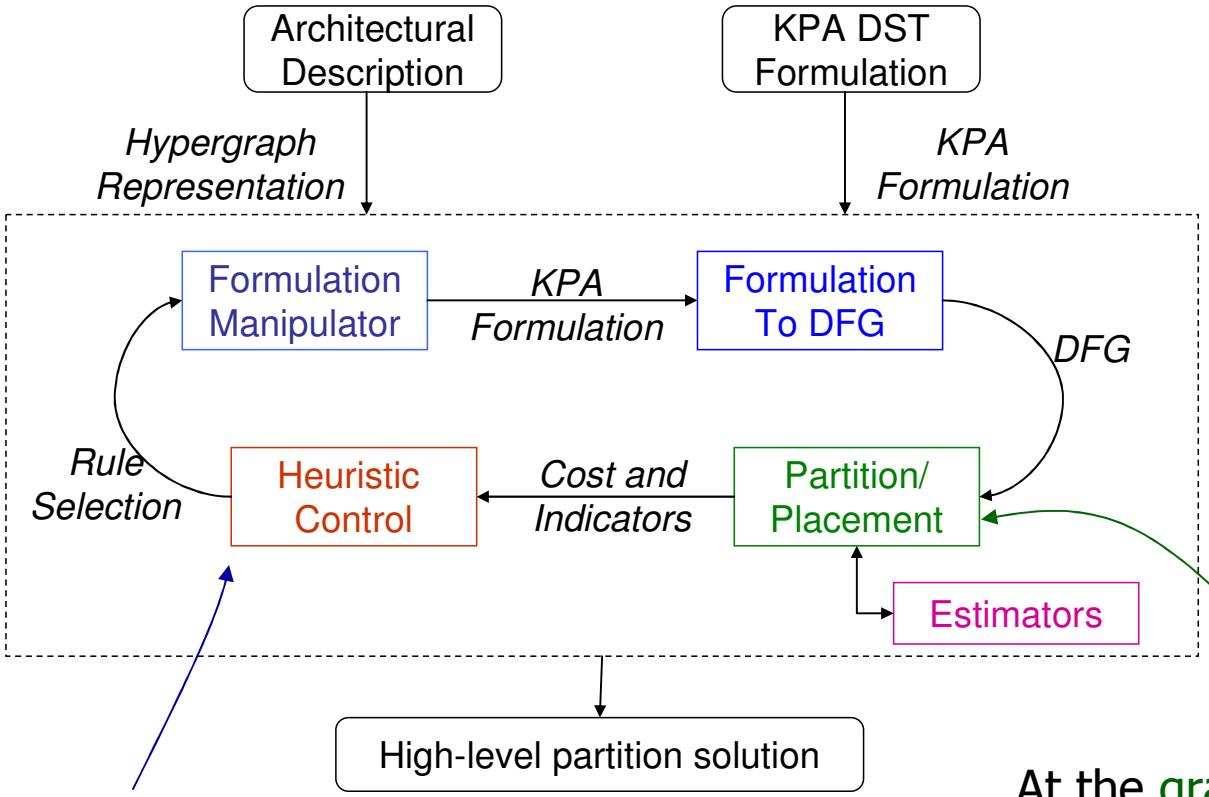
Problem Formulation

Given a Discrete Signal Transform and a description of a distributed hardware architecture, partition the DST by taking advantage of its algorithmic and graphic properties.



Methodology



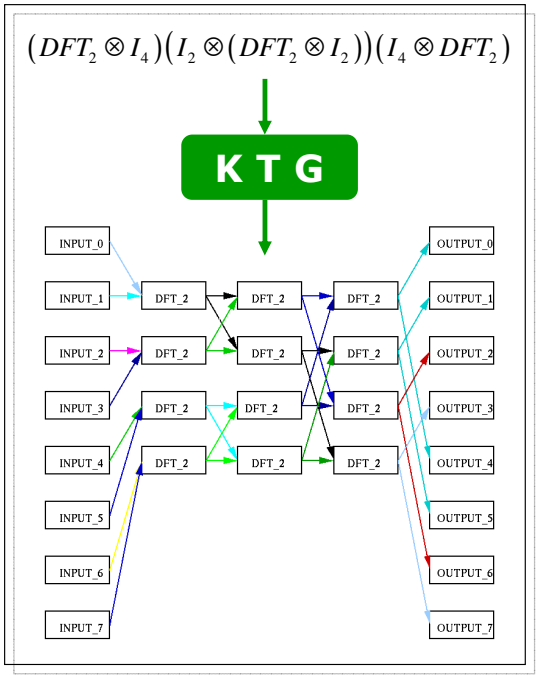
DST-features are introduced in two abstraction levels as part of our methodology: at the **graph level** and the **algorithmic-level**.

At the algorithm-level, an exploration is conducted in search of equivalent transform formulations that are more suitable for the target topology.

At the graph partitioning level, a series of DST-specific structural considerations have been taken to improve the graph partitioning heuristic.

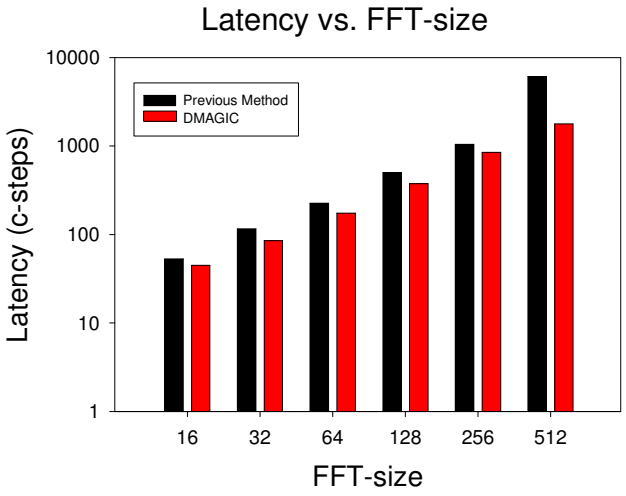
Application Tools

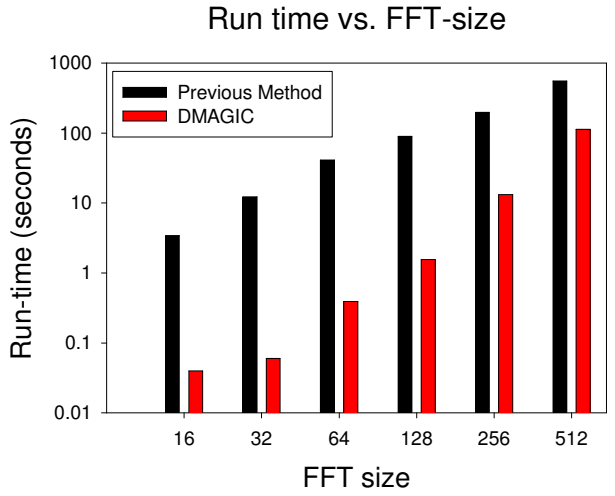
- Conceptual tool - Kronecker Products Algebra (KPA):
  - Compact framework for formulation of DSTs
  - Governed by well known rules and properties
  - Commonly used to explore alternate formulations which better exploit architectural features
  - Formulation 'implies' structure
- Software tools
  - KPA to dataflow graph tool
    Partitioning/placement, resource and latency estimation heuristics adapted to the DST problem
  - Experiments to assess reformulation impact on partition quality



Research Results

- Assessment of algorithmic level transformations effect on partition solution quality.
- Greedy strategy for formulation exploration based on DST factorization.
- Comparison against DFG-based generic HL partitioning tool [Srinivasan01]





- New factorization algorithm for regular fast DCTs.
- Tool for KPA to dataflow graph conversion

Publications

Published & accepted articles in peer-reviewed forums

1. R. Arce Nazario, M. Jiménez, D. Rodríguez. "Partitioning Exploration for Automated Mapping of Discrete Cosine Transforms onto Distributed Hardware Architectures". Accepted to the 50th IEEE Midwest Symposium on Circuits and Systems. August 2007. Montreal, Canada.
2. R.. Arce Nazario, M. Jiménez, D. Rodriguez. "Algorithmic-level Exploration of Discrete Signal Transforms for Partitioning to Distributed Hardware Architectures". Accepted for publication on Journal of IET Computers & Digital Techniques. April 2007.
3. R. Arce Nazario, M. Jiménez, D. Rodríguez. "High-level Partitioning of Discrete Signal Transforms for Multi-FPGA Architectures". 16th IEEE International Conference on Field Programmable Logic and Applications. August 2006. Madrid, Spain.
4. R. Arce Nazario, M. Jiménez, D. Rodríguez. "Functionally-aware Partitioning of Discrete Signal Transforms for Distributed Hardware Architectures". 49th IEEE Midwest Symposium on Circuits and Systems. August 2006. San Juan, PR.
5. R. Arce Nazario, M. Jiménez, D. Rodríguez. "Effects of High-Level Discrete Signal Transform Formulations on Partitioning for Distributed Hardware Architectures". IEEE on Symposium Field-Programmable Custom Computing Machines. April 2006. Napa, CA

Submitted article

1. R. Arce Nazario, M. Jiménez, D. Rodríguez. "Mapping of Discrete Cosine Transforms onto Distributed Hardware Architectures". Submitted to Journal of VLSI Signal Processing. April 2007. Springer.